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DATA SHEET

CBTV4010
10-bit DDR SDRAM mux/bus switch

Product data

2002 Feb 19

File under Integrated Circuits — ICL03

Philips
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10-bit DDR SDRAM mux/bus switch CBTV4010

FEATURES

- Enable signal is SSTL_2 compatible
- Optimized for use in Double Data Rate (DDR) SDRAM applications
- Designed to be used with 400 Mbps/200 MHz DDR data bus
- Switch on resistance is designed to eliminate the need for series resistor to DDR SDRAM
- 20 Ω on resistance
- Internal 100 Ω pull-down resistors
- Low differential skew
- Matched rise/fall slew rate
- Low cross-talk data-data/data-DQM
- Independent DIMM control lines
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

This 10-bit bus switch is designed for 2.3 V to 2.7 V V_{CC} operation and SSTL_2 select input levels.

Each Host port pin is multiplexed to one of four DIMM port pins. When the S pin is low the corresponding 10-bit bus switch is turned on. The on-state connects the Host port to the DIMM port through a 20 Ω nominal series resistance. When the S pin is high the switch is open and a high-impedance state exists between the two ports. The DIMM port is terminated with a 100 Ω resistor to ground when the S pin is high. The design is intended to have only one DIMM port active at any time.

The part incorporates a very low cross-talk design. It has a very low skew between outputs (< 50 ps) and low skew (< 50 ps) for rising and falling edges. The part has optional performance in DDR data bus applications.

Each switch has been optimized for connection to 1 or 2-bank DIMMs.

The low internal RC time constant of the switch (20 Ω × 7 pF) allows data transfer to be made with minimal propagation delay.

The CBTV4010 is characterized for operation from 0 to +85 °C.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	C_L = 7 pF; V_{CC} = 2.5 V	140	ps
C_{IN}	Input capacitance – control pins	V_I = 0 V or V_{CC}	1.8	pF
C_{ON}	Channel on capacitance	V_{in} = 1.5 V	7	pF
I_{CCZ}	Total supply current	V_{CC} = 2.5 V	500	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
TFBGA64 (Thin Fine Pitch BGA)	0 to +85 °C	CBTV4010EE	SOT746-1

64-BALL BGA CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11
A	V_{DD}	$\overline{S1}$	NC		1DP0	2DP0	3DP0		2DP1	3DP1	0DP2
B	$\overline{S2}$	V_{DD}	$\overline{S0}$	GND	0DP0	HP0	0DP1	1DP1	HP1	GND	1DP2
C	NC	$\overline{S3}$								HP2	2DP2
D		GND								3DP2	
E	2DP9	3DP9								0DP3	1DP3
F	1DP9	HP9								HP3	2DP3
G	0DP9	3DP8								GND	3DP3
H		2DP8								0DP4	
J	1DP8	HP8								HP4	1DP4
K	0DP8	GND	HP7	0DP7	3DP6	HP6	GND	3DP5	HP5	3DP4	2DP4
L	3DP7	2DP7	1DP7		2DP6	1DP6	0DP6		2DP5	1DP5	0DP5

NOTE: BLANK SPACE INDICATES NO BALL

SA00589

PIN DESCRIPTION

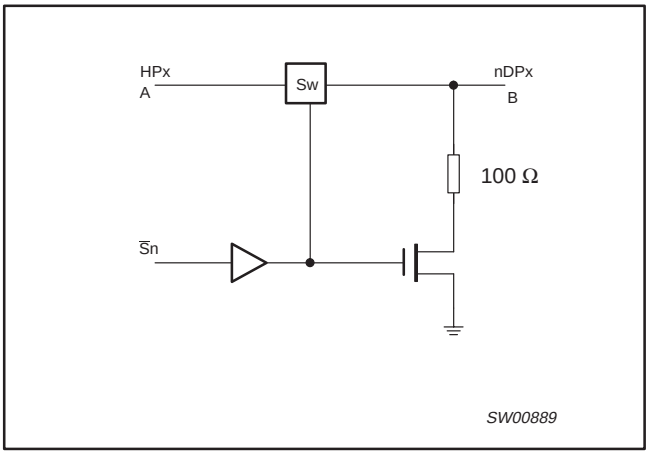
PIN NUMBER	SYMBOL	NAME AND FUNCTION
B6, B9, C10, F2, F10, J2, J10, K3, K6, K9	HP0–HP9	Host ports
A2, B1, B3, C2	S0–S3	Select
A5, A6, A7, A9, A10, A11, B5, B7, B8, B11, C11, D10, E1, E2, E10, E11, F1, F11, G1, G2, G11, H2, H10, J1, J11, K1, K4, K5, K8, K10, K11, L1, L2, L3, L5, L6, L7, L9, L10, L11	0DP0–3DP3 0DP1–3DP1 0DP2–3DP2 0DP3–3DP3 0DP4–3DP4 0DP5–3DP5 0DP6–3DP6 0DP7–3DP7 0DP8–3DP8 0DP9–3DP9	DIMM ports
B10, D2, G10, K2, K7,	GND	Ground
A1, B2	V_{DD}	Positive supply voltage

FUNCTION TABLE

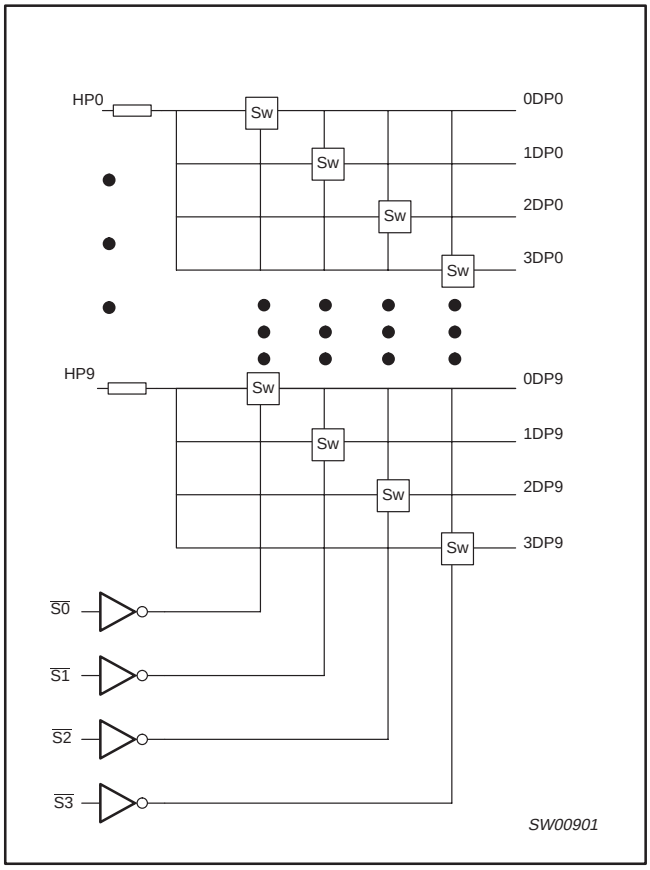
INPUT $\overline{S}$	FUNCTION
L	Host port = DIMM port
H	Host port = Disconnect DIMM port = 100 Ω to GND

H = High voltage level
L = Low voltage level

SIMPLIFIED SCHEMATIC, EACH FET SWITCH



LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1, 3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +3.3	V
I_{IK}	DC input clamp current	$V_{I/O} < 0$	–50	mA
V_I	DC input voltage range ($\overline{S}$ pin only)[2]		V_{CC} + 0.3	V
T_{stg}	Storage temperature range		–65 to 150	°C
V_I	DC input voltage range (except $\overline{S}$ pin)[2]		–0.5 to 3.3	V

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	DC supply voltage	2.3	2.5	2.7	V
V_{IH}	High-level input voltage DIMM port and Host	1.6	—	—	V
V_{IL}	Low-level Input voltage DIMM port and Host	—	—	0.9	V
T_{amb}	Operating free-air temperature range	0	—	+85	°C

NOTE:
1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				T_{amb} = 0 to +85 °C			
				Min	Typ[1]	Max	
V_{IK}	Input clamp voltage	V_{CC} = 2.3 V; I_I = –18 mA		—	—	–1.2	V
I_I	Input leakage current	V_{CC} = 2.5 V; V_I = V_{CC} or GND; $\overline{S}$ = V_{CC}	$\overline{S}$	—	—	±100	µA
			Host port	—	—	±100	
		$\overline{S}$ = GND for $I_{IL\ (test)}$	DIMM port	—	—	±100	
I_{CC}	Quiescent supply current	V_{CC} = 2.5 V; I_O = 0, V_I = V_{CC} or GND		—	0.7	1.5	mA
C_{in}	Control pin capacitance	V_I= 2.5 V or 0		—	1.8	3	pF
C_{on}	Switch on capacitance	V_{in}= 1.5 V		—	—	10	pF
r_{on}[2]	On-resistance	V_{CC} = 2.5 V; V_A = 0.8 V; V_B = 1.0 V		16	20	30	Ω
		V_{CC} = 2.5 V; V_A = 1.7 V; V_B = 1.5 V		16	20	30	

NOTES:
1. All typical values are at V_{CC} = 2.5 V, T_{amb} = 25 °C
2. Measured by the current between the Host and the DIMM terminals at the indicated voltages on each side of the switch.
3. Capacitance values are measured at a of 10 MHz and a bias voltage 3 V. Capacitance is not production tested.

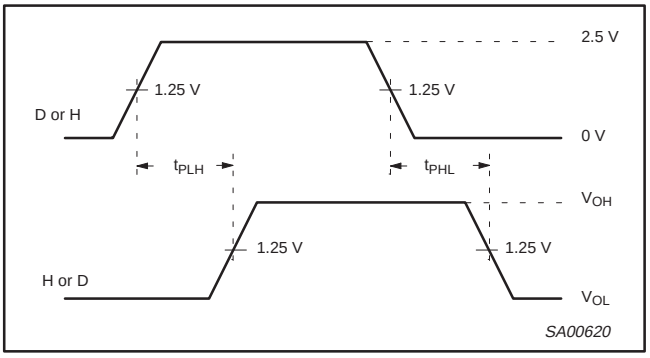
AC CHARACTERISTICS

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = +2.5 V ±0.2 V			UNIT
				Min	Typ	Max	
t_{pd}	Propagation delay[1]	HPx or xDPx	xDPx or HPx	—	—	140	ps
t_{en}	enable	$\overline{S}_n$	HPx or nDPx	1	—	2	ns
t_{dis}	disable	$\overline{S}_n$	HPx or nDPx	1	—	3	ns
t_{osk}	Output skew Any output to any output, Waveform 4 (see note 2)			—	25	50	ps
t_{esk}	Edge skew Difference of rising edge propagation delay to falling edge propagation delay, Waveform 5 (see note 2)			—	25	50	ps

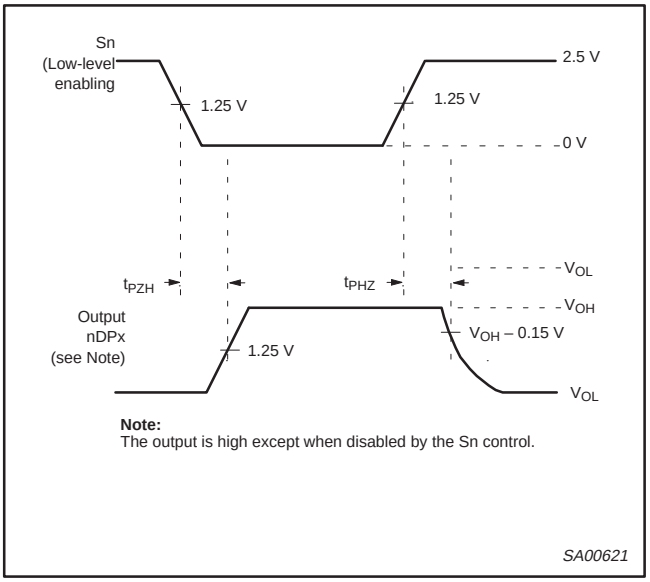
NOTES:
1. The propagation delay is based on the RC time constant of the typical on–state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance); 20 Ω × 7 pF.
   This parameter is not production tested.
2. Skew is not production tested.

HPx to nDPx AC WAVEFORMS AND TEST CIRCUIT

AC WAVEFORMS

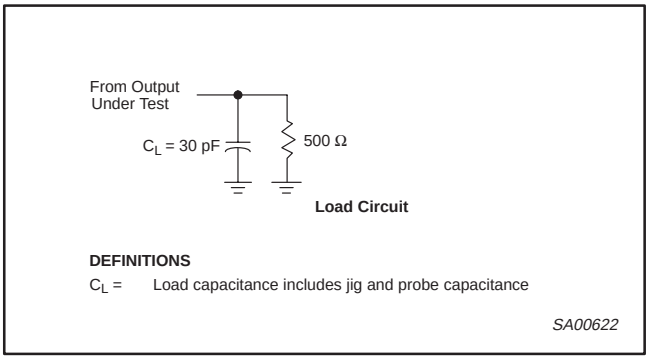


Waveform 1. Input (D or H) to Output (H or D) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT HPx to xDPx

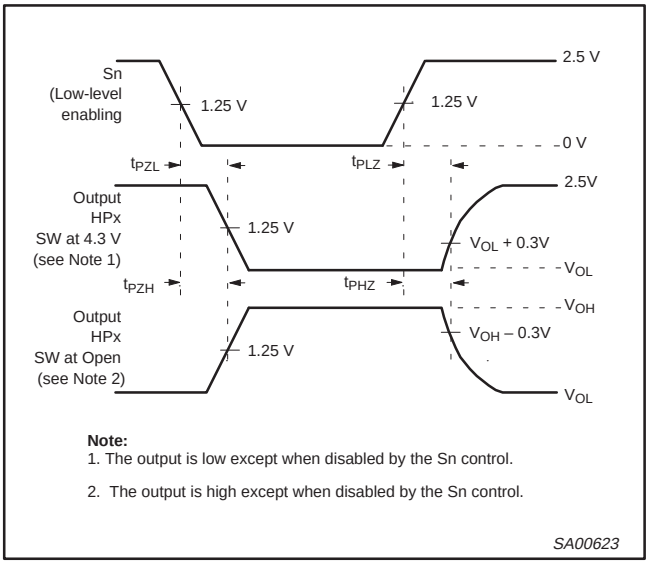


NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
2. The outputs are measured one at a time with one transition per measurement.

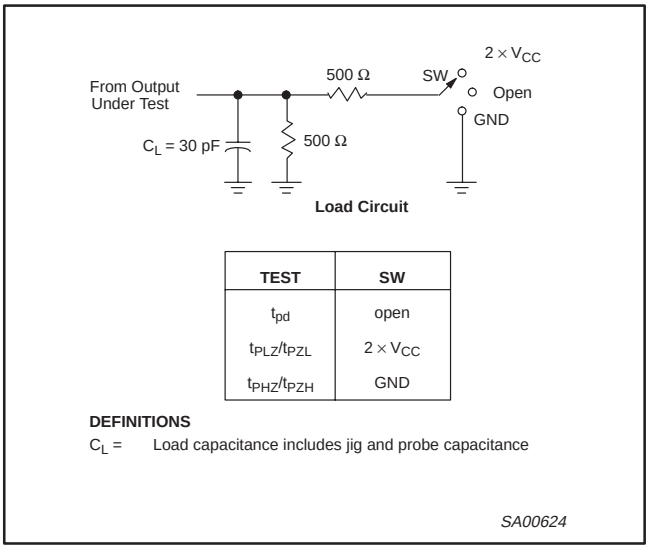
nDPx to HPx AC WAVEFORMS AND TEST CIRCUIT

AC WAVEFORM



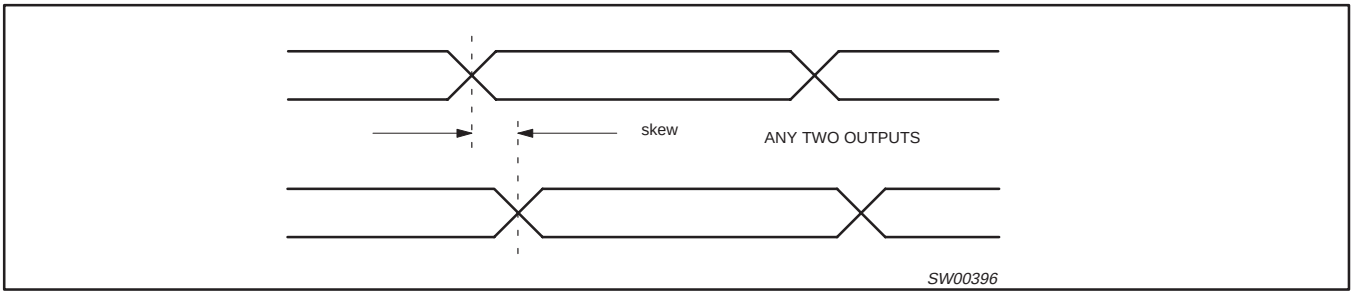
Waveform 3. 3-State Output Enable and Disable Times

TEST CIRCUIT nDPx to HPx

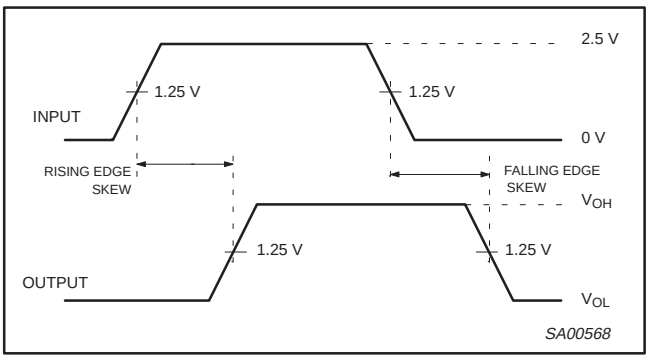


NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
2. The outputs are measured one at a time with one transition per measurement.

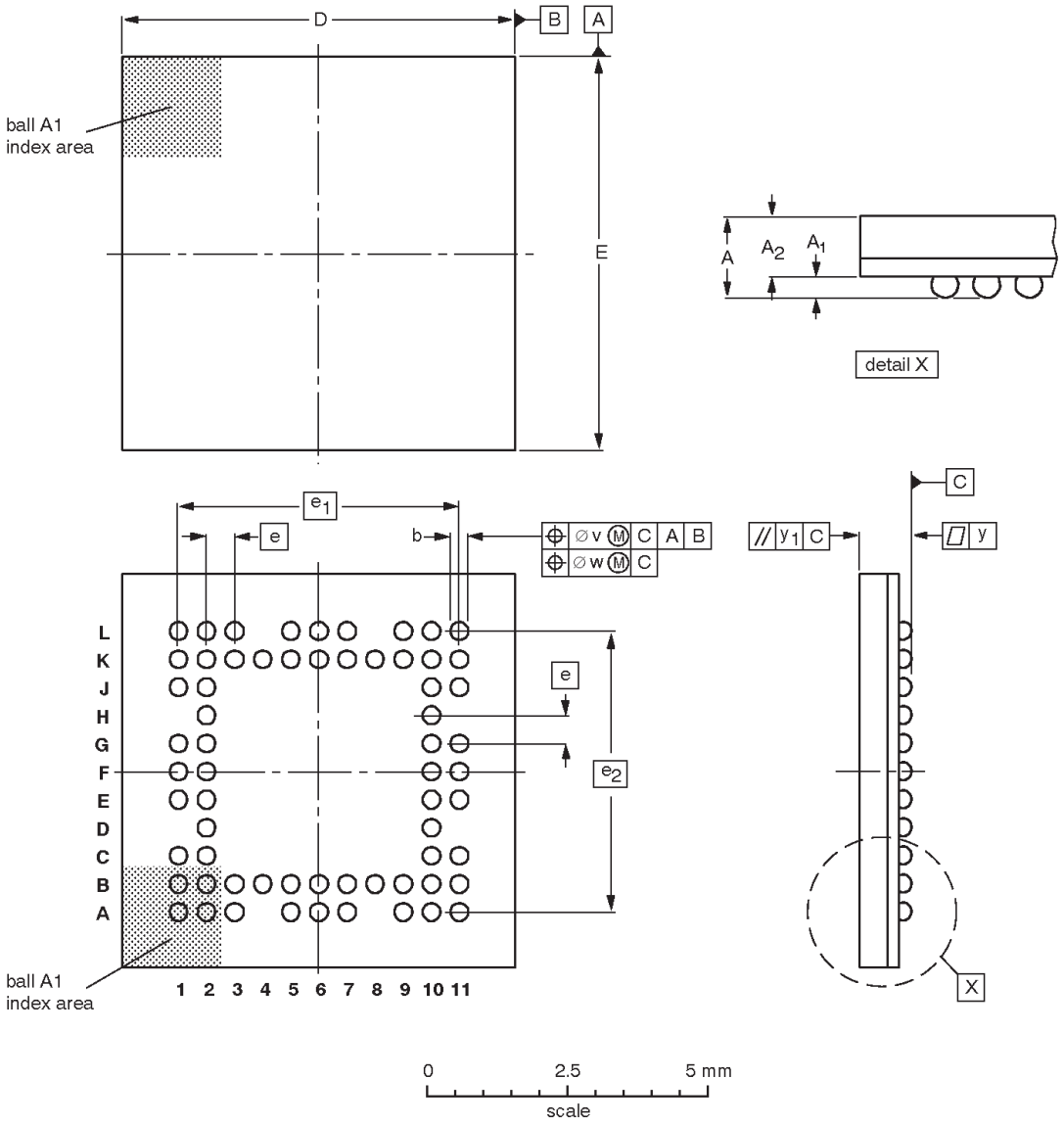


Waveform 4. Skew Between Any Two Outputs



Waveform 5. Rising and Falling Edge Skew

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls; body 7 x 7 x 0.7 mm SOT746-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.3 0.2	0.9 0.6	0.35 0.25	7.1 6.9	7.1 6.9	0.5	5	5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT746-1	- - -	MO-195	- - -			02-01-11

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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